阅读申明

1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描叙上的差异，建议读者做出适当判断。
4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.

2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader’ s learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.

3. All product information provided on the website refer to solutions from manufacturers’ technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.

4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with “Datasheets”.

Cypress Semiconductor Corporation
CY14B104NA 4M nvSRAM Automotive Characterization Report

Design Engineering Director or Manager
David Still
dstl@cypress.com

Product Engineering Director
Jesse Siman
zsj@cypress.com

Product Engineer
Gokul Kumar S
gkus@cypress.com

Applications Engineer
Shivendra Singh
zsk@cypress.com

Marketing Engineer
PK Sidharth
ksi@cypress.com

www.cypress.com

198 Champion Ct.
San Jose, CA 95134 USA

Tel: (408) 943 2600
Fax: (408) 943 4730

1.0 Table of Contents

1.0 Table of Contents 2

2.0 Introduction 3

2.1 General Description 3
2.2 Datasheet 4
2.3 Application Notes 4
2.4 White Papers 4
2.5 Qualification Report 4

3.0 Characterization Hardware and Setup 5

3.1 ATE Characterization Hardware 5
3.2 Characterization Conditions 5

4.0 Characterization Data 6

4.1 DC Parameters 6
4.2 AC Parameters 7
4.3 Store and Recall Parameters 8

Document History Page 9

2.0 Introduction

2.1 General Description

Asynchronous Non RTC

The Cypress CY14B104NA is a fast static RAM (SRAM), with a non-volatile element in each memory cell. The memory is organized as 256K words of 16-bits each. The embedded nonvolatile elements incorporate Quantum Trap technology, producing the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while independent non-volatile data resides in the highly reliable Quantum Trap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power-down. On power-up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

Figure 1: Pin Diagram – 48 ball FBGA (x16)

Figure 2: Pin Diagram – 44TSOPII (x16)

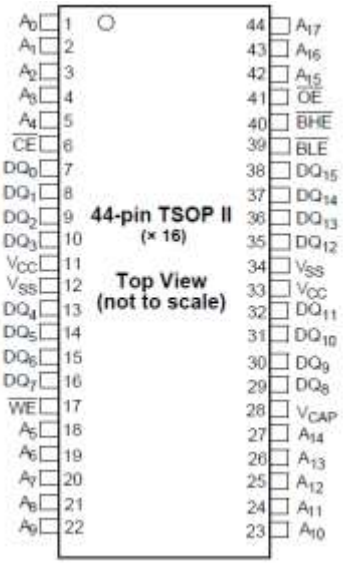
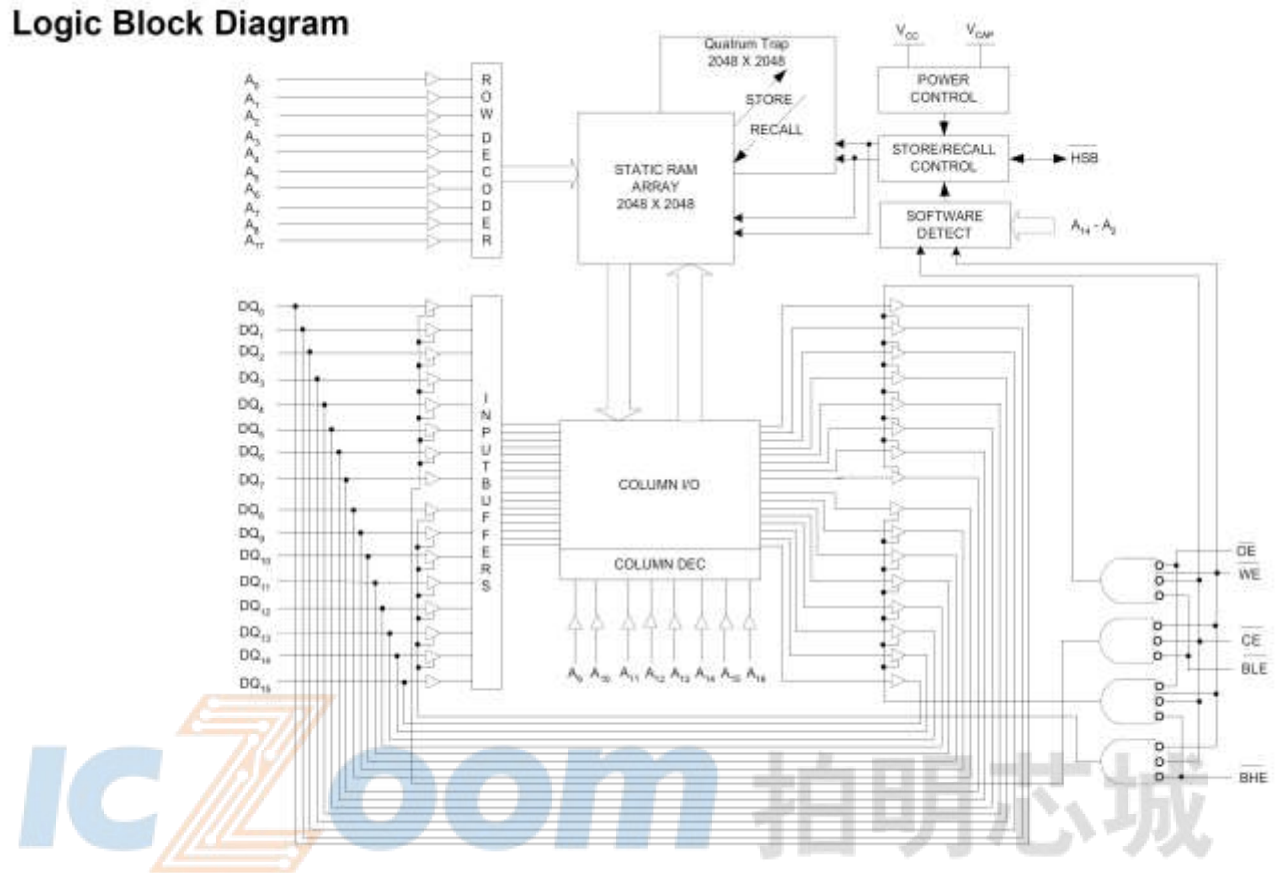


Figure 3: Logic Block Diagram



2.2 Datasheet

The CY14B104NA meets all datasheet specifications for both automotive-A and automotive-E grade devices as per spec 001-54469.

2.3 Application Notes

Following are the application notes associated with CY14B104NA:

- AN 43593 - STORAGE CAPACITOR (VCAP) OPTIONS FOR CYPRESS NVSRAM

2.4 White Papers

Following are the white papers associated with CY14B104NA:

- NONVOLATILE SRAM (NVSRAM) BASICS
- NVSRAM AS WRITE JOURNAL IN RAID STORAGE SYSTEMS

2.5 Qualification Report

The CY14B104NA device is qualified under QTP 163004. The qualification reports are available from the Cypress website at http://www.cypress.com (Specific website URL is TBD).

3.0 Characterization Hardware and Setup

3.1 ATE Characterization Hardware

Temperature Forcing System
The Temptronic XStream 4300 was used to force all the required temperatures.

ATE Testers
Advantest T5581 tester was used to characterize the DC, AC and Store/Recall parameters.

3.2 Characterization Conditions

All units were tested across 2.7V to 3.6V in addition to a +/- 100mV guardband. The temperature range for the characterization was from -40C to 125C. A guardband of +/-5C was used. A total of 90 units were tested for all parameters tabulated. This characterization report compares devices from the FAB4 (SkyWater) which is the old Cypress fab at Minnesota, MN, U.S.A. to the new FAB25 (Cypress) at Austin, TX, U.S.A.

Automotive grade	Temperature range	Voltage range
A	-40C to 85C	2.7V to 3.6V
E	-40C to 125C	3.0V to 3.6V

4.0 Characterization Data

4.1 DC Parameters

Parameter	Name	Test Conditions	Grade	Datasheet			Fab4		Fab25		Unit
				Min	Typ	Max	Min	Max	Min	Max	
ICC1	Average VCC current	tRC = 25 ns, Values obtained without output loads (IOUT = 0 mA)	Auto-A			70	40.40	49.00	39.60	44.40	mA
		tRC = 45 ns Values obtained without output loads (IOUT = 0 mA)	Auto-A			52	32.80	39.60	31.20	35.20	mA
			Auto-E			65	32.80	39.60	24.80	33.60	mA
ICC2	Average VCC current during STORE	All inputs don't care, VCC = Max. Average current for duration tSTORE	Auto-A	-	-	10	3.60	4.20	3.60	6.40	mA
			Auto-E	-	-	15	4.00	4.40	3.20	10.40	mA
ICC3	Average VCC current at tRC=200ns, VCC (Typ), 25 °C	All inputs cycling at CMOS Levels. Values obtained without output loads (IOUT = 0 mA).		-	35	-	25.20	30.00	20.80	29.20	mA
ISB	VCC standby current	CE# > (VCC – 0.2 V). VIN < 0.2 V or > (VCC – 0.2 V). 'W' bit set to '0'. Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.	Auto-A	-	-	5	0.81	1.70	1.08	1.77	mA
			Auto-E	-	-	10	0.81	2.54	0.87	7.48	mA
IIX[2]	Input leakage current (except HSB#)	VCC = Max, VSS < VIN < VCC	Auto-A	-1	-	1	-0.44	0.00	-0.02	0.38	uA
			Auto-E	-5		5	-0.44	0.10	-0.22	0.94	uA
	Input leakage current (for HSB#)	VCC = Max, VSS < VIN < VCC	Auto-A	-100	-	1	-27.38	0.00	-0.08	0.02	uA
			Auto-E	-100		5	-27.38	0.10	-0.02	0.06	uA
IOZL	Off state output leakage current	VCC = VCC(Max), VSS < VOUT < VCC, CE# or OE# > VIH or BLE#, BHE# > VIH or WE# < VIL	Auto-A	-1	-	1	-0.16	0.02	-0.08	0.04	uA
			Auto-E	-5		5	-0.16	0.02	-0.78	0.00	uA
VIH	Input HIGH voltage		Auto-A	2	-	Vcc+0.5	1.67	1.85	1.67	1.74	V
			Auto-E	2.2		Vcc+0.5	1.67	1.85	1.65	1.74	V
VIL	Input LOW voltage			Vss-0.5	-	0.8	0.98	1.14	1.06	1.10	V
VOH	Output HIGH voltage	IOUT=-2mA		2.4	-	-	2.53	2.59	2.46	2.89	V
VOL	Output LOW voltage	IOUT=4mA		-	-	0.4	0.18	0.22	0.06	0.19	V

Notes:
1. These parameters are guaranteed by design but not tested.
2. The HSB pin has IOUT = –2 µA for VOH of 2.4 V when both active HIGH and LOW drivers are disabled. When they are enabled standard VOH and VOL are valid. This parameter is characterized but not tested.

4.2 AC Parameters

Parameter[10]	Name	Datasheet			Fab4		Fab25		Unit
		Min	Typ	Max	Min	Max	Min	Max	
tACE	Chip enable access time	-	-	25	16.30	19.36	15.62	18.87	ns
tAA[1]	Address access time	-	-	25	16.96	20.05	17.17	21.44	ns
tDOE	Output enable to data valid	-	-	12	6.23	7.15	4.88	7.25	ns
tOHA[1]	Output hold after address change	3	-	-	8.10	9.62	6.31	12.56	ns
tDBE	Byte enable to data valid	-	-	12	6.82	7.88	5.38	7.44	ns
tPWE	Write pulse width	20	-	-	8.63	10.56	9.00	12.06	ns
tSCE	Chip enable to end of write	20	-	-	8.44	10.44	8.19	10.94	ns
tAW	Address setup to end of write	20	-	-	12.25	13.62	11.94	15.68	ns
tSA	Address setup to start of write	0	-	-	-8.19	-6.88	-8.18	-6.56	ns
tHA	Address hold after end of write	0	-	-	-11.12	-9.56	-11.50	-9.43	ns
tBW	Byte enable to end of write	20	-	-	10.25	11.19	8.06	11.19	ns

Notes:
1. Device is continuously selected with CE#, OE# and BLE# / BHE# LOW.

4.3 Store and Recall Parameters

AutoStore/Power-UP RECALL Characteristics

Parameter	Name	Grade	Datasheet			Fab4		Fab25		Unit
			Min	Typ	Max	Min	Max	Min	Max	
tHRECALL[1]	Power-Up RECALL duration		-	-	20	15.70	17.20	11.70	18.20	ms
tSTORE[2]	STORE cycle duration		-	-	8	5.40	6.60	4.60	7.60	ms
tDELAY[3]	Time allowed to complete SRAM write cycle		-	-	25	19.00	19.00	19.00	19.00	ns
VSWITCH	Low voltage trigger level	Auto-A	-	-	2.65	2.48	2.60	2.40	2.49	V
		Auto-E	-	-	2.95	2.42	2.60	2.40	2.49	V

Software Controlled STORE and RECALL Characteristics

Parameter [4,5]	Name	Datasheet			Fab4		Fab25		Unit
		Min	Typ	Max	Min	Max	Min	Max	
tSA	Address setup time	0	-	-	-4.56	-3.69	-4.50	-2.75	ns
tCW	Clock pulse width	20	-	-	7.88	8.69	6.88	9.56	ns
tHA	Address hold time	0	-	-	-5.13	-4.31	-4.93	-2.87	ns
tRECALL	RECALL duration	-	-	200	70.00	85.00	55.00	110.00	us

Hardware STORE Characteristics

Parameter	Name	Datasheet			Fab4		Fab25		Unit
		Min	Typ	Max	Min	Max	Min	Max	
tDHSB	HSB# to output active time when write latch not set	-	-	25	17.00	18.00	17.00	18.00	ns
tPHSB	Hardware STORE pulse width	15	-	-	3.00	4.50	4.00	4.70	ns
tSS[6,7]	Soft sequence processing time	-	-	100	60.00	70.00	50.00	90.00	us

Notes:
1. tHRECALL starts from the time VCC rises above VSWITCH.
2. If an SRAM write has not taken place since the last NV cycle, no AutoStore or Hardware STORE takes place.
3. On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time tDELAY.
4. The software sequence is clocked with CE# controlled or OE# controlled reads.
5. The six consecutive addresses must be read in the order listed. WE# must be HIGH during all six cycles.
6. This is the amount of time it takes to take action on a soft sequence command. VCC power must remain HIGH to effectively register command.
7. Commands such as STORE and RECALL lock out I/O until complete which further increases this time.